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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,093	03/23/2004	Amar Guettaf	1875.4450000	1879
26111	7590	04/18/2006	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			RADOSEVICH, STEVEN D	
			ART UNIT	PAPER NUMBER
			2138	
DATE MAILED: 04/18/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/806,093	GUETTAF, AMAR
	<b>Examiner</b>	<b>Art Unit</b>
	Steven D. Radosevich	2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 23 March 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-28 is/are rejected.  
 7) Claim(s) 1,4,8,10,13-17,20-22 and 25-28 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 23 March 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

Claims 1-28 are present for examination.

### ***Priority***

Acknowledgement is made that no priority either foreign or domestic is claimed for this application and as such the filing date (3/23/2004) is being used for this examination.

### ***Information Disclosure Statement***

Acknowledgement is made that no Information Disclosure Statement (IDS) was provided with the application.

### ***Drawings***

The drawings (Figures 1, 2, and 5) are objected to by the examiner for improper or lack of directional arrows indicating data flow direction. Specifically figure 1 has improper directional arrows indicating data output which conflicts with the known data flow direction of the electrical components (MUX and flip-flops) within the figure. Examiners recommendation that applicant reverse the direction of the improper directional arrows in Figure 1 to correspond to the correct data flow direction (such as 132C - "To output contact point" and "To integrated circuit input" in figure 1) to overcome this rejection. Examiner also recommends adding directional arrows to figures 2 and 5 for consistency in the figures specifically to indicate the flow of data direction through the Scan Paths (200, 220, 240, 500, 520, 540, 560) for clear understanding of the figures and to overcome this rejection. Appropriate correction is required in these figures.

### ***Claim Objections***

Claim 1 is objected to because of the following informalities: There is a grammatical error in line 7 of the claim. For purposes of examination the Examiner interprets that scan tests are conducted "on" not "of" the plurality of scan paths. Appropriate correction is required.

Further, Claim 1 is objected to since in step "(e)" of the claim it is unclear to the examiner what is being traced in the instance wherein a "good scan path" outputs the number of errors indicative of no errors (i.e. zero). Appropriate correction or explanation is required.

Further, Claim 1 is objected to since in step "(f)" of the claim it is unclear to the examiner how the "good scan paths" provide any information relevant to the shifting of the segment point and returning to step "(b)" to additionally segment the single identified bad scan path already segmented into two segments. Appropriate correction or explanation is required.

Claims 4 and 20 are objected to because of the following informalities: There is a grammatical error in line 2 of each claim. For purposes of examination Examiner interprets that scan tests are conducted "on" not "for" the plurality of scan paths. Appropriate correction is required.

Claims 8 and 21 are objected to since it is unclear to the examiner how the two segments are equal in size after step "(b)" and "(c)" ("i" in this examination) respectively wherein the segment point has been shifted and there is a return to the segmentation

step "(b)" and "(c)" ("I" in this examination) respectively. For purposes of examination Examiner interprets that only the initial segmentation segments of the scan path segmented can be of equal size, any movement of the segment point at which future segmentation is to be done would result in the two segments being unequal in size. Appropriate correction is required.

Claims 10 and 22 are objected to because of the following informalities: It is unclear to the examiner after reading the specification what applicant is referring to when incorporating "a coupled error source" in line 4 of the claim. Appropriate correction or explanation is required.

Claims 13-16 and 25-28 are objected to because of the following informalities: It is unclear to the examiner which "end" (claims 13 and 25 line 3, claims 14 and 26 line 2, or "beginning" (claims 15 and 27 line 5, claims 16 and 28 line 2) the applicant is referring to when establishing a location for the segment point. Examiner notes that a scan chain has two defined ends or two beginnings. Appropriate correction or explanation is required.

Claim 17 is objected to because of the following informalities: There is a grammatical error in line 8 of the claim. For purposes of examination the Examiner interprets that scan tests are conducted "on" not "of" the plurality of scan paths. Appropriate correction is required.

Further, Claim 17 is objected to since in step "(f)" ("I" in this examination) of the claim it is unclear to the examiner what is being traced in the instance wherein a "good

scan path" outputs the number of errors indicative of no errors (i.e. zero). Appropriate correction or explanation is required.

Further, Claim 17 is objected to since in step "(g)" ("m" in this examination) of the claim it is unclear to the examiner how the "good scan paths" provide any information relevant to the shifting of the segment point and returning to step "(c)" ("i" in this examination) to additionally segment the single identified bad scan path already segmented into two segments. Appropriate correction or explanation is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the bad scan path and good scan paths" in lines 8-9. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is no prior reference to "good scan paths" since there has only been identifying of a single "bad scan path" (line 4) in the claim, all other scan paths are yet to have been identified as being anything other than a scan paths.

Further, Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner acknowledges that the applicant segments the identified bad scan path in line 6 of the claim 1. Examiner notes that the

segmentations serve no purpose in the invention as it has been claimed since only the scan paths in their entirety are examined thereafter.

Claim 2 recites the limitation "good scan paths" in lines 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is no prior reference at the point in which this claim is dependent upon of "good scan paths" since, there has only been identifying of a single "bad scan path" (line 4 of claim 1), all other scan paths are yet to have been identified as being anything other than a scan path. This claim may not be further considered on its merits since examiner interprets it only pertains to the "good scan paths" not yet established.

Claim 17 recites the limitation "the bad scan path under test and good scan paths" in lines 9-10. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is no prior reference to "good scan paths" since there has only been identifying of a single "bad scan path" (line 6) and "bad scan paths" (line 4) in the claim, all other scan paths are yet to have been identified as being anything other than a scan paths.

Further, Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner acknowledges that the applicant segments the identified bad scan path in line 7 of the claim 1. Examiner notes that the segmentations serve no purpose in the invention as it has been claimed since only the scan paths in their entirety are examined thereafter.

Further, Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner acknowledges that the applicant wishes to return to a step in line 17 of the claim. However, the step in which the applicant wishes to return to is not indicated within the claim. For the purposes of this examination the examiner is treating the step returned to as being that of "(b)" in the instant application ("h" in this examination) since this step follows the characteristic of step "(b)" from claim 1 of the instant application.

Claim 18 recites the limitation "good scan paths" in lines 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is no prior reference at the point in which this claim is dependent upon of "good scan paths" since, there has only been identifying of a single "bad scan path" (line 6) and "bad scan paths" (line 4) in the claim, all other scan paths are yet to have been identified as being anything other then a scan path. This claim may not be further considered on its merits since examiner interprets it only pertains to the "good scan paths" not yet established.

Claims 2-16 are dependent on claim 1 and therefore also inherits 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

Claim 3 is dependent on claim 2 and therefore also inherits 35 U.S.C. 112, second paragraph issues of the claim and may not be further considered on its merits.

Claims 18-28 are dependent on claim 1 and therefore also inherits 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

Claim 19 is dependent on claim 18 and therefore also inherits 35 U.S.C. 112, second paragraph issues of the claim and may not be further considered on its merits.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-4, 10-20, and 22-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Martin-de-Nicolas (2003/0208710).

1. As per claim 1, Martin-de-Nicolas teaches scan testing of an integrated circuit with a plurality of scan paths, a method of debugging scan testing failures of the integrated circuit, comprising the steps of:

- a. Identifying a bad scan path that is generating one or more errors within the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19);
- b. Segmenting the bad scan path into two segments (0028 and 0031);
- c. Conducting scan tests of the plurality of scan paths (0019 line 9);

- d. Assessing scan test results on the bad (0018 lines 8-10 and 0022 lines 16-19);
- e. Tracing the source of errors when the number of errors of an output of the bad scan path are less than a bad path error threshold (0018 lines 10-12 and 0029); and
- f. Shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan path and returning to step (b) when the number of errors of an output of the bad scan path are greater than a bad path error threshold (0028-0029 and 0031).

Examiner interprets that applicant is claiming simply a binary search to identify and locating errors within a bad scan chain. Martin-de-Nicolas teaches throughout his publication such a binary search for locating errors or faults within scan chains.

- 2. As per claims 2 and 18, Martin-de-Nicolas teaches that all the scan paths are tested a number of times with multiply tests confirming which scan paths are faulty and which are not (0019 line 7-9 in addition to 0022 lines 15-19).
- 3. As per claims 3 and 19, the art is replete with masking of identified faulty scan paths while further testing any remaining unidentified scan paths as faulty with various tests. This method of masking reduces processing time since the identified faulty scan paths are not retested or examined since they are already found to be faulty (0019 lines 7-9).

4. As per claim 4, Martin-de-Nicolas teaches wherein step (a) of claim 1 includes running a series of scan tests for the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19).
5. As per claims 10 and 22, Martin-de-Nicolas teaches wherein in step (e) of claim 1 and (f) ("I" in this examination) the tracing of errors includes identifying a first error source that generated an error and determining whether the error originated with the first error source (0029). Examiner interprets that "identifying a first error source," is the determining of the location of the error, that error must have originated within "the first error source," since it was identified as the first error source.
6. As per claims 11 and 23, Martin-de-Nicolas teaches wherein the tracing the source of errors is conducted manually (0005 lines 1-3).
7. As per claims 12 and 24, Martin-de-Nicolas teaches wherein the tracing the source of errors is conducted automatically through an automated testing unit (0008).
8. As per claims 13-16 and 25-28, Martin-de-Nicolas teaches the sifting of the segment point midway or in the direction from its present location to the end/beginning of the scan chain dependent on the testing results (0028-0029 and 0031). Examiner notes that this is the implementation of a binary search for locating errors or faults such as taught throughout the publication by Martin-de-Nicolas.
9. As per claim 17, Martin-de-Nicolas teaches scan testing of an integrated circuit with a plurality of scan paths, a method of debugging scan testing failures of the integrated circuit, comprising the steps of:

- g. Identifying a plurality of bad scan paths that is generating one or more errors within the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19);
- h. Masking all bad scan paths except a bad scan path under test (0019 lines 7-9);
- i. Segmenting the bad scan path into two segments (0028 and 0031);
- j. Conducting scan tests of the plurality of scan paths (0019 line 9);
- k. Assessing scan test results on the bad (0018 lines 8-10 and 0022 lines 16-19);
- l. Tracing the source of errors when the number of errors of an output of the bad scan path under test are less than a bad path error threshold (0018 lines 10-12 and 0029); and
- m. Shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan path and returning to step when the number of errors of an output of the bad scan path under test are greater then a bad path error threshold (0028-0029 and 0031).
- n. Repeating steps (b) ("h" in this examination) through (g) ("m" in this examination) until the source or sources of errors within all dad scan paths among said plurality of bad scan paths have been located 0033 lines 6-8).

Examiner interprets that applicant is claiming simply a binary search to identify and locating errors within a bad scan chains. Martin-de-Nicolas teaches throughout his publication such a binary search for locating errors or faults within scan chains.

10. As per claim 20, Martin-de-Nicolas teaches wherein step (a) of claim 17 ("g" in this examination) includes running a series of scan tests for the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas (2003/0208710) as applied to claim 1 above, and further in view of Applicant Admitted Prior Art (AAPA).

11. As per claims 5-7, Martin-de-Nicolas teaches the above as per claim 1 wherein a number of testes are executed on a plurality of scan paths (0019 lines 7-9 with in addition to 0022 lines 16-19).

Martin-de-Nicolas does not specifically teach wherein these tests executed include varying the temperature of the integrated circuit, frequency of a clock signal input, or the test voltage.

However, as evidenced by the AAPA within the specification of the instant application it was known at the time the invention was made when factors such as frequency, temperature, or voltage are changed, errors within that circuit can be caused (0006).

Therefore, the Examiner interprets that the plurality of tests run by Martin-de-Nicolas incorporates these factors of varying the temperature, frequency, and test voltage, wherein these factors are within the limitations in which the circuit is rated to operate since Martin-de-Nicolas desires as does the applicant to identify and locate errors within a DUT (0008, 0019 lines 7-9 with 0029 lines 5-9).

Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas (2003/0208710) as applied to claim 1 above, and further in view of Widmer (6978416).

12. As per claims 8 and 21, Martin-de-Nicolas teaches the above as per claim 1 and 17 respectively wherein a binary search is performed to locate the errors or failures.

Martin-de-Nicolas does not specifically teach wherein performing the binary search the initial segmented segments are of equal size.

However in an analogous art Widmer teaches in performing a binary search that the initial segmentation segments are of equal size.

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine Martin-de-Nicolas' teaching of a binary search by adding Widmer's teaching that in performing a binary search the initial segmented segments are of equal size in-order to as indicated by Widmer quickly determine the location of the errors (column 10 lines 52-55). Examiner notes that continuously segmenting a selected segment under test into equal segments in an effort to locate something such as errors is the basic principle of a binary search and that binary searches were well known in the art at the time the invention was made.

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas (2003/0208710) as applied to claim 1 above, and further in view of Akita (5541940) or Sugimoto et al. (6999386).

13. As per claim 9, Martin-de-Nicolas teaches the above as per claim 1 wherein a binary search is performed to locate the error or failure.

Martin-de-Nicolas does not specifically teach wherein in step (d) there is included a determination of the number of errors generated by the bad scan path.

However in the analogous arts of both Akita and Sugimoto it is taught that it is important to determine the number of errors generated from a DUT.

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the binary search as taught by Martin-de-Nicolas by adding to it determining of the number of errors generated by a DUT as taught by either Akita or Sugimoto so that a determination of weather or not the number

of errors exceeds the capacity of the system may be made and so that all detected errors are located if the number of errors falls within the capacity of the system to do so.

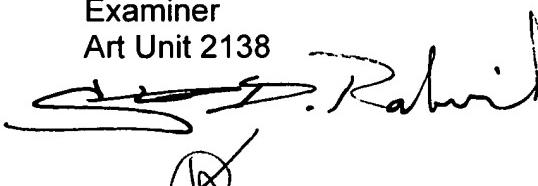
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich  
Examiner  
Art Unit 2138



GUY LAMARRE  
PRIMARY EXAMINER